RESEARCH ARTICLE OPEN ACCESS

To Implement Energy Efficient of Integer Unit by Higher Voltage Flip Flop Based on Minimum operating Dual Supply Voltage Techinque

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Abstract
To achieve the most energy-efficient operation, this brief presents a circuit design technique for separating the power supply voltage (VDD) of flip-flops (FFs) from that of combinational circuits, called the higher voltage FF (HVFF). Although VDD scaling can reduce the energy, the minimum operating voltage (VDDmin) of FFs prevents the operation at the optimum supply voltage that minimizes the energy, because the VDDmin of FFs is higher than the optimum supply voltage. In HVFF, the VDD of combinational logic gates is reduced below the VDDmin of FFs while keeping the VDD of FFs at their VDDmin. This makes it possible to minimize the energy without power and delay penalties at the nominal supply voltage (1.2 V) as well as without FF topological difications. A four bit alu is designed in these paper by using dual supply voltage usig DSCH.
Index Terms—Minimum operating voltage, subthreshold circuits, variations.

I. INTRODUCTION

Power dissipation is a limiting factor in both high-performance and mobile applications. Independent of application, desired performance is achieved by maximizing operating frequency under power constraints that may be dictated by battery life, chip packaging and or cooling costs. Lowering supply voltage results in a quadratic reduction in power dissipation but significantly impacts delay. In constant-throughput applications, This performance loss is recovered by increased Pipelining or parallelism [11, but it increases the latency of the design product values and reduced system-level power without incurring robustness degradation or significant area increase over a conventional flip-flop.

II. 2.PREVIOUS METHOD

As VDD is reduced, the dynamic energy decreases quadratically with VDD.Therefore, the total energy has its minimum value, and VDD at which the energy is minimized is typically around 0.3 V in a logic circuit . Thus, this voltage is the target for energy-efficient LSIs

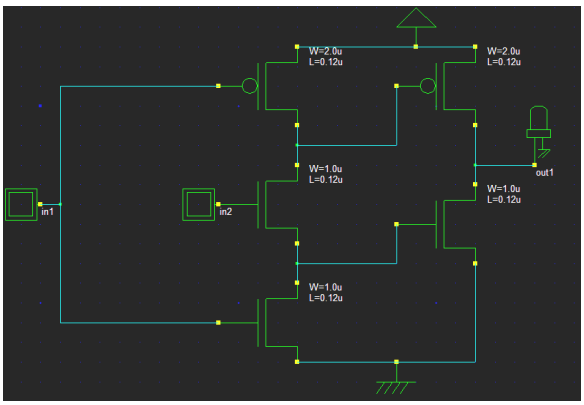
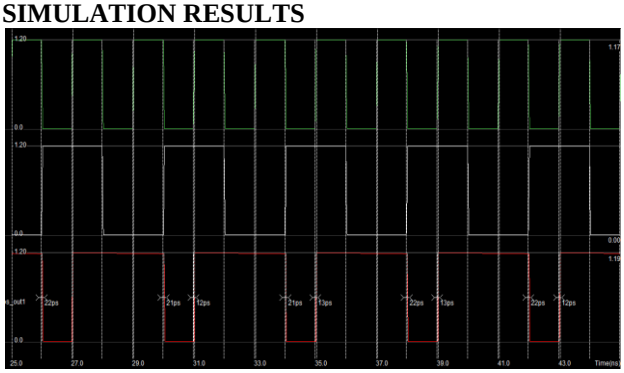


Fig:block diagram of single supply voltage flip flop

SIMULATION RESULTS



Timing diagram of single supply voltage flip flop
Single supply voltage power reduction =3.973 micro wats

III. DUAL-SUPPLY DESIGN

3.1 Optimal VDDL Selection

A theoretical model to investigate power reduction via CVS is proposed in [3]. We employ this top-down approach to determine the VDDL/VDDH ratio for LCFF optimization and comparisons. By using parameters for 0.13pm technology, the optimal VDDL is found to sit between 60% and 70% of VDDH regardless of path delay distribution shapes. The latter value is chosen for higher noise immunity of VDDL signals against VDDH noise.

3.2 Dual-VDD CVS Simulation

A Perl-script-based simulator is implemented to estimate power reduction of a dual-VDD CVS system. As illustrated in Fig. 1, the simulator models the initial single-VDD design as a series of paths each of which consists of a chain of fanout-of-four (F04) inverters (IV) sandwiched between two flip-flops. Three different logic depths - 12, 20, and 40 F04 IV unit delays - are employed to evaluate their impact on power saving of a CVS system initially, all flip-flops and IVs are VDDH cells. The first step substitutes all VDDH flip-flops with LCFFs. Since all LCFFs investigated are driven by a VDDL-swing clock, this substitution can reduce clocking power significantly [121. For negative slack paths caused by the increased delay of LCFFs, the VDDH IVs are equivalent capacitive load connected to the output of each VDDH upsized to maintain the original clock cycle time. The F03- IV remains unchanged. Then, VDDH IVs are replaced with VDDL IVs in each non-critical path until positive slack disappears. This to build the CVS structure. Finally, the simulator calculates the final result.

Power of the CVS structure and compares it with the power of the replacement proceeds in reverse order from the end of each path 0) initial single-VDD design. The impact of different LCFFs and possible using a theoretical approach [3]. Different logic depths on power saving

3. 3 *V*DDmin OF FFS AND HVFF

To estimate the *V*DDmin of FFs, the dependence of the functional failure rate of a single FF on *V*DD is obtained by Monte Carlo SPICE simulations (5000 trials) with with in die threshold voltage variation*)*.When *PF (V*DD(FF*))* is defined as the failure rate of a single FF at *V*DD(FF*)*, the *V*DDmin of *N*-gate FFs can be expressed as

$$\left(1 - P_F\left(V_{\mathrm{DDmin}}\right)\right)^N = Y \qquad (1)$$

$$\Leftrightarrow V_{\mathrm{DDmin}} = P_F^{-1}\left(1 - Y^{\frac{1}{N}}\right) \qquad (2)$$

where *N* is the number of FFs and *Y* is the yield. As shown in Fig. 3, *PF (V*DD(FF*))* is derived from the dependence of the simulated failure rate on *V*DD*(*FF*)* by extrapolation, and the *V*DDmin of FFs is calculated from (2) using *PF (V*DD(FF*))*. For example, the *V*DDmins of 50 and 5000 FFs are estimated to be 432 and 514 mV, respectively, when the yield *Y* is 99%.

These estimated *V*DDmins are much higher than the most energy-efficient supply voltage of around 0.3 V. In conventional circuits with a single power supply, all logic gates must operate at the *V*DDmin of FFs despite the fact that combinational logic gates can operate at a supply voltage much lower than the *V*DDmin of FFs, which prevents the energy reduction achieved by *V*DD scaling. Thus, the energy can be further reduced, if different supply voltages between FFs and combinational circuits are supplied.

PROPOSED METHOD

In this brief, higher voltage FF (HVFF), which is a VDDmin- aware circuit design technique for separating the VDD of FFs from that of combinational circuits, is proposed**.**

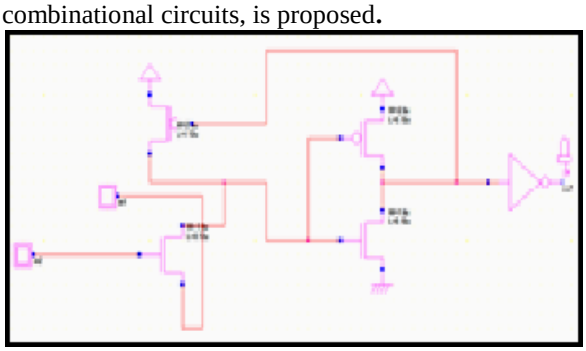
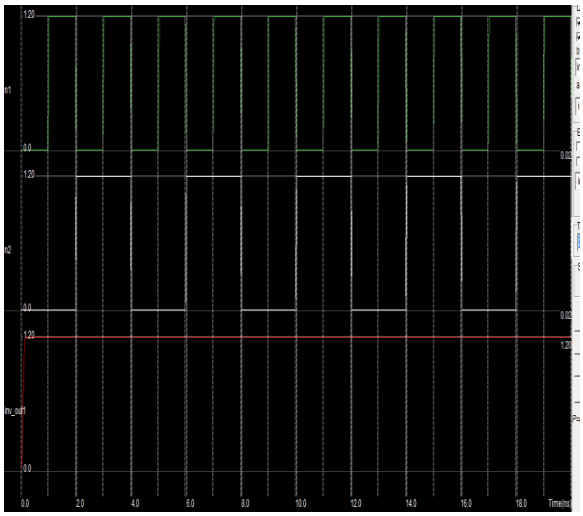


Fig:block diagram of dual supply voltage flip flop

SIMULATION RESULTS

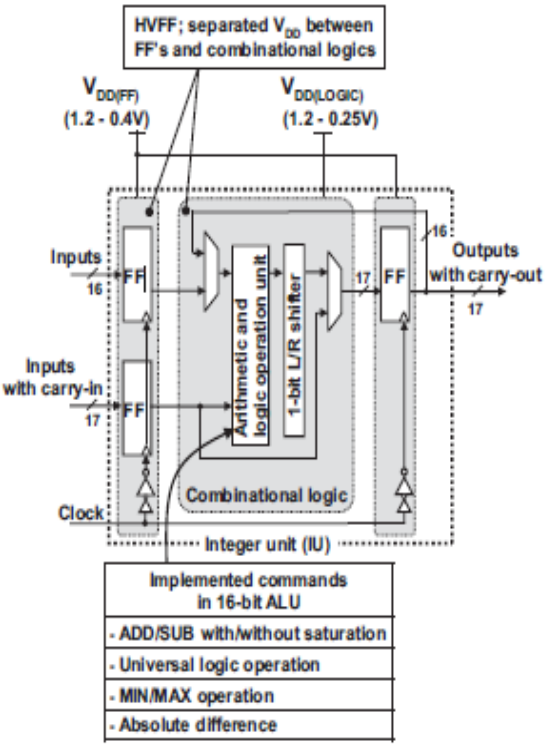


Timing diagram of dual supply voltage flip flop
Dual supply voltage power reduction=0.313mw

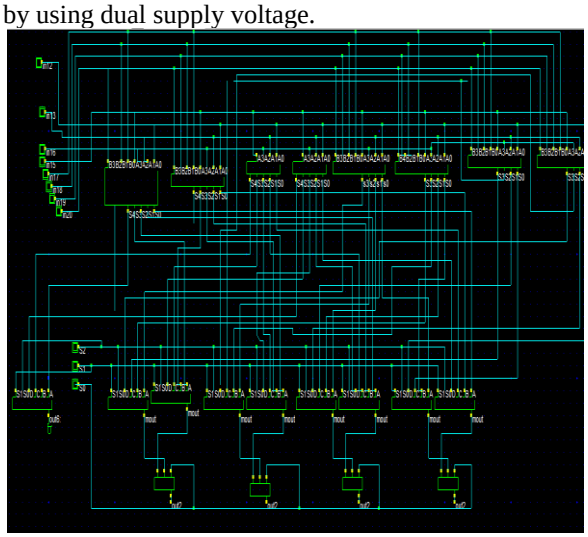
On the other hand, it is possible that the voltage difference between FFs and combinational circuits worsens the *V*DDmin of FFs without level converters. Fig. 4 shows the dependence of the failure rate of a single FF on the supply voltage of combinational logic gates *V*DD*(*LOGIC*)*, when

VDD(FF) is kept at the *VDDmin* of FFs. The lines represent the fitted *PF* (failure rate) curves. If *PF* increases, the *VDDmin* of FFs.

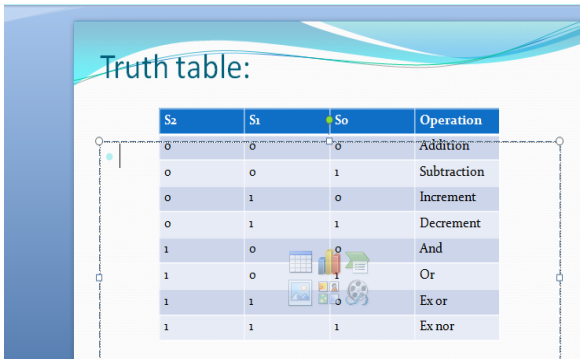
IV. EXPERIMENTAL RESULTS



rises according to (2). In Fig. 4, however, the *PF* curves do not increase even if *VDD(*LOGIC*)*s are reduced by 100 and 140 mV when *VDD(*FF*)*s are 432 and 514 mV, respectively.we implement the 4bit alu by using dual supply voltage.



Truth table:



This indicates that level converters are not required if the voltage difference between FFs and combinational circuits is around 100 mV. When *VDD(*FF*)* is 514 mV (in the case of 5000 FFs), the energy of combinational circuits is reduced by at most 47%. It should be noted that the *VDDmin* of combinational circuits is not considered in this discussion, since it is much lower than that of FFs, as shown in Fig. 1. If HVFF technique is applied to random logic circuits, where FFs are used for other than inputs and outputs of circuits, such as processor cores, the delay and power overheads would become larger.

V. CONCLUSION

To achieve the most energy-efficient operation, HVFF, which is a *VDDmin*-aware circuit design technique for separating the *VDD* of FFs from that of combinational circuits, was proposed. In HVFF, the *VDD* of combinational logic gates is reduced below the *VDDmin* of FFs while keeping the *VDD* of FFs at their *VDDmin* to reduce the energy, since the *VDDmin* of FFs is much higher than that of combinational logic gates. HVFF was applied to a 16-bit IU. The measurement results in a 120-nm CMOS process showed that HVFF can reduce the minimum energy by 13% compared with conventional operation, which is 1/10 times smaller than the energy at the nominal supply voltage, without power and delay penalties at the nominal supply voltage, as well as without FF topological modifications.

REFERENCES

[1] A. W. Wang, B. H. Calhoun, and A. P. Chandrakasan, *Sub-Threshold Design for Ultralow Power Systems*. New York: Springer-Verlag, 2006.

[2] H. Kaul, M. Anders, S. Mathew, S. Hsu, A. Agarwal, R. Krishnamurthy, and S. Borkar, "*A 320mV 56 μW 411 GOPS/Watt ultralow voltage motion estimation accelerator in 65 nm CMOS*," in *IEEE Int. Solid- State Circuits Conf. Dig. Tech. Papers*, Feb. 2008, pp. 316–317.

[3] Y. Pu, J. P. Gyvez, H. Corporaal, and H. Yajun, "*An ultralow energy/frame multi-standard JPEG co-processor in 65 nm CMOS with sub/near-threshold power supply*," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2009, pp. 146–147.

[4] H. Kaul, M. A. Anders, S. K. Mathew, S. K. Hsu, A. Agarwal, R.K. Krishnamurthy, and S. Borkar, "*A 300 mV 494 GOPS/W reconfigurable dual-supply 4-way SIMD vector processing accelerator in 45 nm CMOS*," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2009, pp. 260–261.

[5] A. Agarwal, S. K. Mathew, S. K. Hsu, M. A. Anders, H. Kaul, F. Sheikh, R. Ramanarayanan, S. Srinivasan, R. Krishnamurthy, and S. Borkar, "*A 320 mV-to-1.2 V on-die fine-grained reconfigurable fabric for DSP/media accelerators in 32 nm CMOS*," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2010, pp. 328–329.

[6] J. Kwong, Y. Ramadass, N. Verma, M. Koesler, K. Huber, H. Moormann, and A. Chandrakasan, "*A 65 nm sub-Vt microcontroller with integrated SRAM and switched capacitor DC-DC converter*," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 115–126, Jan. 2009.

[7] B. H. Calhoun and A. P. Chandrakasan, "*Ultradynamic voltage scaling (UDVS) using sub-threshold operation and local voltage dithering*," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 238–245, Jan. 2006.

[8] T. Yasufuku, S. Iida, H. Fuketa, K. Hirairi, M. Nomura, M. Takamiya, and T. Sakurai, "*Investigation of determinant factors of minimum operating voltage of logic gates in 65-nm CMOS*," in *Proc. Int. Symp. Low Power Electron. Design*, Aug. 2011, pp. 117–122.

[9] H. Fuketa, S. Iida, T. Yasufuku, M. Takamiya, M. Nomura, H. Shinohara, and T. Sakurai, "*A closed-form expression for estimating minimum operating voltage (VDDmin) of CMOS logic gates*," in *Proc. Design Autom. Conf.*, Jun. 2011, pp. 984–989.

[10] T. Yasufuku, K. Hirairi, Y. Pu, Y. F. Zheng, R. Takahashi, M. Sasaki, H. Fuketa, A. Muramatsu, M. Nomura, H. Shinohara, M. Takamiya, and T. Sakurai, "*245% power reduction by post-fabrication dual supply voltage control of 64 voltage domains in VDDmin limited ultralow voltage logic circuits*," in *Proc. Int. Symp. Quality Electron. Design*, 2012, pp. 586– 591.

AUTHORS

First Author -- M.Subhashini,received her Bachelor of Technology in Electronics and Communication Engineering in Avr&Svr Engineering College, Nandyal. Her Research To implement energy efficient of integer unit by higher voltage flip flop based on minimum operating dual supply voltage technique using CMOS Technology under the guidance of S.Rambabu.

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